IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SILICONIX INCORPORATED, a Delaware corporation,

Plaintiff,

v.

DENSO CORPORATION, a Japanese corporation, and TD SCAN (U.S.A.), INC., a Michigan corporation,

Defendants.
_____/

AND CONSOLIDATED ACTIONS
NOS. C 04-00344 WHA AND
C 05-03617 WHA.
_____/

No. C 05-01507 WHA

CLAIM CONSTRUCTION ORDER

INTRODUCTION

This is the claim-construction order for United States Patent No. 5,034,785, asserted herein by plaintiff Siliconix incorporated.[1] This order addresses the four disputed phrases selected by the parties. A technology tutorial, full briefing and a *Markman* hearing preceded this order.

[1] Plaintiff spells "incorporated" without a capital I.

STATEMENT

Siliconix is a manufacturer of power MOSFETs (metal-oxide-semiconductor, field-effect transistors). Power MOSFETs regulate the electrical power for many products of the modern age including cell phones, computers, televisions and cars.

An earlier patent involving the technology at issue, United States Patent No. 4,767,722, entitled "Method for making Planar Vertical Channel DMOS Structure," claimed the *methods* of making a particular type of semiconductor device, a DMOS (double diffused metal oxide semiconductor) transistor with a vertical gate and a planar surface. The purported improvement in the '722 patent was that this method provided a flat surface for all masking steps thereby facilitating the manufacture of multiple DMOS transistors. The '722 patent is currently being reexamined before the United States Patent and Trademark Office. The '722 patent is also owned by Siliconix.

In turn, the '785 patent, entitled "Planar Vertical Channel DMOS Structure," claimed *devices* produced by using the methods described in the '722 patent. The '785 patent was a continuation-in-part of an abandoned divisional of the '722 patent. Accordingly, the '785 patent shared a virtually identical specification and figures with the '722 patent. The only major difference was the addition of a Figure 10 and a paragraph describing this figure.

According to plaintiff, the "invention" contained in the '785 patent was that the MOSFET cell contains a "substantially planar top surface" and that the cell's gate is submerged in an insulating layer of dielectric material.[2] Plaintiff maintains that these unique structural features of the '785 deviced produce several corresponding benefits compared to prior-art MOSFETs including: (1) lower on-resistance[3], (2) reduced cell size, (3) manufacturing efficiency, and (4) increased processing yields. Defendants counter that the purportedly unique structural features of the '785 were already disclosed by the prior art, and that those prior-art references already disclosed devices with these positive qualities and efficiencies.

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[2] The "gate" is the switch in the MOSFET cell that controls the flow of current.

[3] "On-resistance" is the resistance of a MOSFET to the flow of current through the device when the device is in the "on" state. Greater on-resistance leads to heat build-up, potentially causing the MOSFET to burnup.

Siliconix has pursued litigation relating to the '722 and '785 patents in this Court before. In October 2003, Siliconix sued Alpha and Omega Semiconductor, Inc. for infringement of these two patents (Case No. C 03-04803 (WHA)). In September 2004, this Court issued an order construing six phrases used in the patents' claims. That order is of some relevance here, as the parties ask the Court to construe some of the same phrases construed in the September 2004 order. That earlier action ultimately settled. Defendants herein, however, were not parties in that case. They must be allowed a *de novo* opportunity to make their case.

In the instant series of consolidated actions, Siliconix only claims infringement of the '785 patent. The defendants are Denso Corporation, TD Scan (U.S.A.), Matsushita Electric Industrial Co., Ltd., Panasonic Corporation of North America, and Advanced Analogic Technologies, Inc. ("AATI"). All of the defendants except AATI are companies that purchase power MOSFETs for use in their automotive, industrial and electronic products. AATI manufactures competing power MOSFETs.

ANALYSIS

Claim construction is a matter of law to be decided by a judge, not a jury. *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 388 (1996). Since the September 2004 order, the Federal Circuit has offered a clarification of the legal principles of claim construction in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), *cert. denied*, 126 S. Ct. 1332 (2006). As explained in *Phillips*, courts must give words in the claims their ordinary and customary meaning, which "is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Id.* at 1312–13. Where this ordinary and customary meaning is not immediately clear, courts must primarily look to intrinsic evidence (*i.e.*, the claims, the specification and the prosecution history) to determine the meaning. *Id.* at 1314. With respect to the specification, although a difficult task, a court must distinguish "between using the specification to interpret the meaning of a claim and importing limitations from the specification into the claim." *Id.* at 1323. The latter is never permissible.

Although courts have the discretion to consider extrinsic evidence, including expert and inventor testimony, dictionaries and scientific treatises, *Phillips* made clear that such evidence

is "less significant than the intrinsic record in determining the legally operative meaning of claim language." *Id*. at1317 (citation omitted). "The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction." *Id*. at 1315.

The *Phillips* opinion, however, reaffirmed "that there is no magic formula or catechism for conducting claim construction." *Id*. at 1324. "Nor is the court barred from considering any particular sources or required to analyze sources in any specific sequence, as long as those sources are not used to contradict claim meaning that is unambiguous in light of the intrinsic evidence." In other words, "[t]he sequence of steps used by the judge in consulting various sources is not important; what matters is for the court to attach the appropriate weight to be assigned to those sources in light of the statutes and policies that inform patent law." *See also Pfizer, Inc. v. Teva Pharm. USA, Inc.*, 429 F.3d 1364, 1374–75 (2005); *Old Town Canoe Co. v. Confluence Holdings Corp.*, __ F.3d __, 2006 WL 1228887, at *5 (Fed. Cir. May 9, 2006).

* * *

Though the parties disagree over many terms in the patent in suit, they have jointly selected four disputed terms or phrases to be construed at this time. They are: (1) "substantially coplanar," (2) "substantially planar top surface," (3) "means for electrically contacting the top surface of said third region," and (4) "electrically conductive region."

1. "SUBSTANTIALLY COPLANAR"

The phrase "substantially coplanar" appeared in independent claims 1, 14 and 15 of the '785 patent. For example, claim 1 stated (col. 6, line 50–col. 7, line 9) (emphasis added):

> 1. A vertical gate semiconductor device comprising:
> a drain region of a first conductivity type;
> a body region of a second conductivity type opposite said first conductivity type overlaying said drain region, said body region having a first portion and a second portion, said second portion having a first top surface;
> a source region of said first conductivity type overlaying said first portion of body region and having a second top surface **substantially coplanar** with said top surface, said source region being separated from said drain region by said body region;
> a first dielectric region defining a groove extending

> downward through said source and said body regions and into said drain region;
> a gate region disposed in said groove and having a top surface depressed with respect to said second top surface of said source region, said gate region filling said groove at least up to a bottom of said source region;
> a second dielectric region having a substantially planar top surface overlaying said gate region, the top surface of said second dielectric region being **substantially coplanar** with said first and second top surfaces; and
> an electrically conductive region electrically contacting said source and body regions.

Likewise, claim 14 in pertinent part provided for "an insulating layer formed over said gate structure, said insulating layer being **substantially coplanar** with the top surface of said third region" (col. 8, lines 40–43) (emphasis added). Claim 15 described "a second insulating layer formed over said gate structure, said second insulating layer being **substantially coplanar** with a top surface of said second plurality of semiconductor regions" (col. 9, lines 7–10) (emphasis added).

Siliconix contends that "substantially coplanar" means "lying largely on the same plane." In contrast, defendants propose that this phrase be construed as "forming one essentially flat (planar) surface."

In the September 2004 order, this phrase was construed consistently with Siliconix's proposed definition—"lying largely in the same plane" (Order at 9–10). Defendants argue that the previous construction was performed under an outdated claim-construction standard articulated in *Texas Digital Systems, Inc. v. Telegenix, Inc.*, 308 F.3d 1193, 1202–04 (Fed. Cir. 2002), *cert. denied*, 123 S. Ct. 2230 (2003).

It is true that the September 2004 order discussed extrinsic dictionary evidence prior to discussing the specification and prosecution history when construing "substantially coplanar." Yet as stated above, the *sequence* of analysis of the varying types of evidence is not what is important. What *is* important is whether the proper weight is ascribed to each type of evidence. *Phillips* reiterated that courts must determine the meaning that most naturally aligns with the patent's description of the invention. Dictionary evidence is still acceptable provided it is "not an improper attempt to find meaning in the abstract divorced from the context of the intrinsic

record but properly was a starting point in its analysis, which was centered around the intrinsic record." *Old Town Canoe*, 2006 WL 1228887, at *5.

Ordinarily "coplanar" means "lying or acting in the same plane." Merriam-Webster, *Ninth New Collegiate Dictionary* (1984). This is precisely how the phrase was used in the patent.

The claim language clearly suggests that the phrase "substantially coplanar" was used to describe the relative location of different layers and surfaces. That is, "coplanar," unlike "planar," is a comparative word describing the *relationship* of two surfaces or regions rather than simply describing one surface in isolation. On this straightforward reading, one of ordinary skill in the art would view coplanar as it is commonly used, describing two objects on the same plane.

In turn, the word "substantially" has been consistently read by the Federal Circuit to mean "largely but not wholly that which is specified." *LNP Eng'g Plastics, Inc. v. Miller Waste Mills, Inc.*, 275 F.3d 1347, 1354 (Fed. Cir. 2001); *see also Liquid Dynamics Corp. v. Vaughan Co.*, 355 F.3d 1361, 1368 (Fed. Cir. 2004) ("words of approximation, such as 'generally' and 'substantially' are not descriptive terms commonly used in patent claims 'to avoid a strict numerical boundary to the specified parameter"). The specification bears this interpretation out.

On a plain-language reading, two "substantially coplanar" surfaces, as in claim 1, or surfaces and layers as in claims 14 and 15, are "lying largely in the same plane." As explained in the September 2004 order (Order at 10):

> Both Claims 14 and 15 require the insulating layer to be "substantially coplanar" with the top surface of the source region. As discussed above, the specification does not require absolute flatness of the surface. The diagrams in the specification show that the top surface is not absolutely flat with surface of the source region. Thus, the term "substantially coplanar" does not require the two different regions to be on the exact same plane as to create a geometrically contiguous flat surface.

The specification supports this plain-meaning reading of the claim limitations. Defendants rely on the specification's description of Figure 4f pictured here (col. 4, lines 44–49):

> The wafer is then oxidized in an atmosphere containing oxygen (which consumes a portion of polysilicon layer 33 in groove 31*) until the top surface of the oxidized portion 35 above gate 34 forms an essentially flat (planar) surface with the top surface of passivating layer 30.

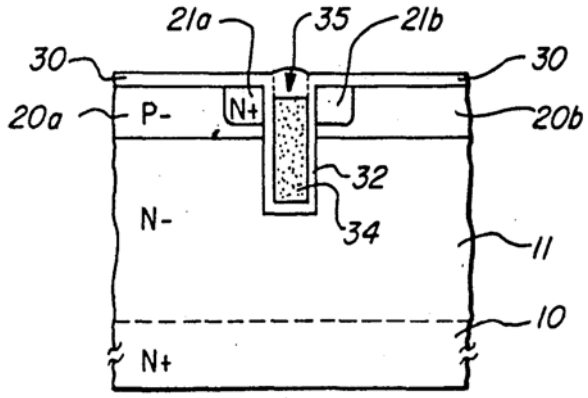


Figure 4f (slightly modified).

Nothing about this passage, however, suggests an idiosyncratic definition of "*coplanar*," but rather of "*planar*." This passage did not use the contested phrase, nor did the specification at any point. Moreover, Figure 4f, shown here, was only a diagram of the MOSFET cell in the process of fabrication—not a completed cell. This is important because the claims using the phrase "substantially coplanar" all described *completed* devices not preliminary devices created in the fabrication process. Finally, the graphic representation in Figure 4f did not look as defendants suggest it did. Rather, the top surface of the oxidized portion (35) was at most depicted as lying primarily on the same plane as the top surface of the passivating layer (30)—the figure did not depict the two top surfaces as fused.

Likewise, Figure 3, shown here, depicted an embodiment of the '785 invention that suggests a plain-meaning reading of "substantially coplanar." Siliconix categorizes Figure 3 as the "*preferred* embodiment," a categorization challenged by defendants. Regardless if

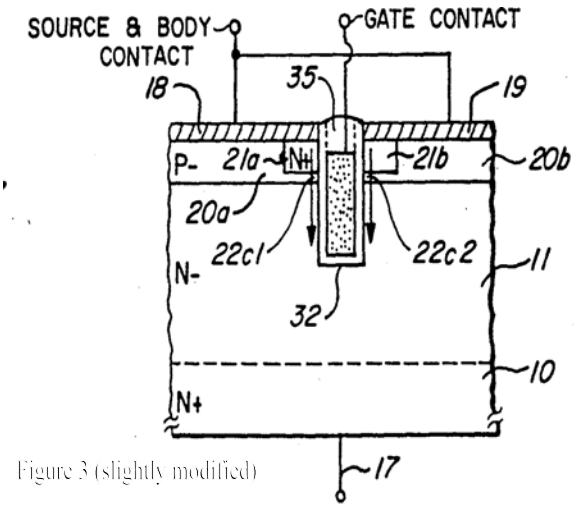


Figure 3 (slightly modified)

Figure 3 encapsulated the *preferred* embodiment, or just one of several possible embodiments, Figure 3 showed that the '785 inventor intended to use "substantially coplanar" in its ordinary sense. Figure 3 showed "one embodiment of the vertical gate planar DMOS power transistor of the present invention" (col. 3, lines 17–19). This embodiment did not show the two top surfaces of layers 35 and 19 forming one surface layer. Rather, the top surfaces of these layers are mostly on one plane, without being fused. Moreover, Figure 3, unlike Figure 4f, depicted a completed cell.

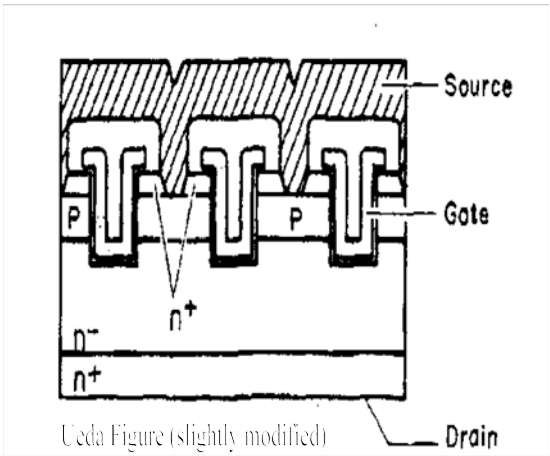
Defendants rely on the term "depressed" in claim 1 for a textual argument that Figure 3 cannot be an embodiment of the '785 invention. Claim 1 indicated that the top surface of the gate region was "depressed" in relationship to the top surface of the source region (col. 6, line 67). Figure 3 depicted the substantially coplanar top surface of the dielectric region and the top surfaces of the source and body regions as being further apart than the top surface of the gate region from the top surface of the source region. If the term "depressed" meant anything, it is argued, it must have indicated a greater deviation than "substantially coplanar." There is no support, however, for this conjecture in the '785 specification. It is a conclusory argument that "depressed" must signify a greater deviation than "substantially coplanar." This argument is particularly unpersuasive given the inventor's use of the modifier "substantially." Figure 3 could have embodied the scope of deviation permissible for "*substantially* coplanar." This argument is too attenuated to alter the remainder of the analysis in this order.

According to defendants, the prosecution history disclaimed Siliconix's proposed definition of substantially coplanar. In turn, it is argued, Figure 3 cannot be an embodiment of the '785 invention because it depicted two surfaces only mostly on the same plane.

It is true that the prosecution history contains a pattern of modifications by the '785 inventor to increase the claimed degree of flatness of the invention. The patent examiner rejected the '785 application on several occasions as being anticipated by prior art references. One such prior art reference was U.S. Patent No. 4,630,088 ("the Ogura reference"). In response, the inventor ratcheted up the flatness of the claimed invention in order to distance the invention from the prior art. Unlike the Ogura reference, the inventor pointed out that the '785

device contained "a gate region fills the groove at least up to the source region which, in cooperation with other structural features of Applicant's invention, achieves a substantially planar top surface overlaying the gate region" (Saros Decl. Exh. F at 35871).

Coplanarity and planarity, however, are different attributes, despite the shared root word. The patent examiner did not reject the '785 application on grounds that its degree of coplanarity was anticipated by the prior art. And the inventor did not add the element of coplanarity in the claims in response to an examiner's action. "Coplanar" was in claims 14 and 15 from the outset of the application, and one use of "coplanar" was already in claim 1 at the time of the application. The modifications made by the inventor were to the flatness or planarity of the claimed device. With respect to the relationship of the surfaces and regions, however, the limitations remained the same. The different surfaces and layers were depicted and described as bearing a relation described by the ordinary meaning of "coplanar." When modified by "substantially," it is clear that devices such as that depicted in Figure 3 fit the ultimate claims of the '785 patent.



Ueda Figure (slightly modified)

The same is true with respect to the inventor's distinguishing of "the Ueda prior-art reference." During the prosecution, the inventor distinguished the '785 technology from the prior art as follows (Saros Decl. Exh. F at 35862) (emphasis added):

> Claim 15 distinguishes from Applicant's Figure 2, *inter alia*, in that Figure 2 does not have an electrically conductive region overlaying a dielectric region which in turn overlays the gate region, the dielectric region having top surface *substantially coplanar* with top surfaces of the source and body regions.

The figure described in this passage is a prior-art reference of an industry article from 1985 by Daisuke Ueda of defendant Matsushita (*id*. at Exh. G). According to defendants, unless "substantially coplanar" meant "forming one unified layer," the '785 application was anticipated by the Ueda reference. Again, this is not so. The Ueda prior-art figure, shown here, did not depict an insulating layer largely on the same plane as the body or source regions *at all*.

The coplanarity of the regions was simply not a feature of the Ueda reference. An insulating layer lying largely on the same plane as the source and body regions as depicted in Figure 3 of the '785 patent, *supra*, thus would not necessarily have been anticipated by the Ueda reference. Although the inventor may have increased the claimed flatness to get around the Ueda reference, the inventor did not disclaim any particular scope of coplanarity.

Viewing all of the intrinsic evidence, and the extrinsic evidence in the context of the intrinsic evidence, this order construes "substantially coplanar" as "lying largely in the same plane."[4]

2. "SUBSTANTIALLY PLANAR TOP SURFACE"

The phrase "substantially planar top surface" only appeared in claim 1 of the '785 patent, although the phrases "planar" and "top surface" appeared throughout the patent. As stated above, claim 1 provided for (col. 7, lines 3–7) (emphasis added):

> a second dielectric region having a **substantially planar top surface** overlaying said gate region, the top surface of said second dielectric region being substantially coplanar with said first and second top surfaces. . . .

Siliconix proposes that "substantially planar top surface" should be construed as "largely as flat as practicable" with "top surface" having its ordinary meaning. Defendants propose that this contested phrase means "a top surface that is essentially flat."

This Court construed the use of "planar" in the earlier '722 patent in the September 2004 order. That order concluded that "planar means as flat as practicable" (Order at 3). As noted, these two patents share virtually the same specification and the '785 application arose out of the '722 patent. This order, however, finds that the constructions of the two patents in this context must be different given that the '785 patent describes a *device* whereas the '722 patent describes a *method*.

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[4] This construction does not rely on the expert testimony of W. Milton Gosney, submitted by Siliconix. As explained in this Court's December 2005 case management order, expert testimony is useful during claim construction, if at all, to address points outside of the intrinsic record necessary for proper construction. Here, the expert testimony is not necessary. Under *Phillips*, this order must rely more heavily on the intrinsic record than on extrinsic evidence prepared exclusively for the purposes of litigation. 415 F.3d at 1317.

The starting point for the construction of this disputed phrase is the '785 specification's use of a parenthetical in providing that "the top surface of the oxidized portion 35 above gate 34 forms an essentially flat (planar) surface" (col. 4, lines 40–43). By the use of this parenthetical, the inventor clearly equated "planar" and "flat." As stated above, unlike "coplanar" above, "planar" did not describe the relative locations of surfaces. Rather "planar" described a single flat surface.

It is true, as plaintiff notes, that the figures in the '785 patent consistently depicted "planar" surfaces that were not entirely flat. Consider, for example, Figures 3 and 4f, *supra*. It may be, as defendants suggest, that considering the scale of the figures, these deviations from perfect flatness are minuscule. Nevertheless, one skilled in the art would recognize that such minor deviations occur and that a description of the surface of a MOSFET as planar would take these deviations into account.

Nevertheless, the '785 patent strived for optimal flatness. The device would have the greatest functionality with the greatest degree of flatness—the device would be best as a perfectly flat surface. The device patent thus supports a construction that limits the patent to nearly perfect flatness without reference to the practicalities of the production.

The prosecution history supports a reading of "planar" that requires nearly perfect flatness. The '785 inventor distinguished the Ogura reference, *supra*, by noting that in the '785 invention "a gate region fills the groove at least up to the source region which, in cooperation with other structural features of Applicant's invention, achieves a substantially planar top surface overlaying the gate region" (Saros Decl. Exh. F at 35871). Based on this statement, the '785 patent's planarity must be construed in a way that separates it from the prior-art patent. Again, the figures in the prosecution history (and ultimate patent) show that even ideally planar surfaces may contain minor bumps consistent with the limitations of planarizing top surfaces. Nevertheless, the '785 patent's improvement over the prior art, according to the inventor himself, was its flatness. Indeed, when following the history of the '785 it becomes clear that the inventor had to repeatedly claim the device as more and more flat to address repeated

rejections by the patent examiner. "Planar," therefore, must be interpreted as signifying such precise flatness.

As stated above, the term "substantially" has been construed under Federal Circuit precedent and by this Court to mean "largely." Here, however, the '785 specification itself provided a synonym for "substantially" in the context of planarity. As quoted above, that phrase was "essentially" (col. 4, lines 40–43). This order, therefore, finds that "essentially" is the best construction of "substantially."

Finally, the September 2004 order did not further construe "top surface" because it found its ordinary meaning was straightforward. "Top surface" need not be construed, as the parties apparently agree, as the ordinary meaning of "top surface" will be evident to the jury. *See, e.g., U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997).

Accordingly, this order construes "substantially planar top surface" to mean "a top surface that is essentially flat."[5]

3. "MEANS FOR ELECTRICALLY CONTACTING THE TOP SURFACE OF SAID THIRD REGION"

The phrase "means for electrically contacting the top surface of said third region" appeared in claim 14 of the '785 patent (col. 8, lines 24–46) (emphasis added):

> 14. A vertical MOS transistor comprising a plurality of cells, each cell comprising:
> a first region of semiconductor material of a first conductivity type;
> a second region of semiconductor material of a second conductivity type formed on said first region;
> a third region of said first conductivity type formed on said second region;
> a groove extending through said third and second regions, said groove extending at least down to said first region;
> a gate structure formed within said groove but insulated from said first, second and third regions, said gate structure completely filling at least the portion of said groove extending below a bottom of said third region;
> an insulating layer formed over said gate structure,

[5] This construction also does not rely on the expert testimony submitted by Siliconix. Rather, the intrinsic evidence guides this construction. The expert declaration is particularly suspect here, given that during Siliconix's litigation against AOS, the same expert, contrary to his current opinion, submitted a declaration that "planar" meant "essentially flat," the construction now adopted in this order.

> said insulating layer being substantially coplanar with the top surface of said third region ;
> **means for electrically contacting the top surface of said third region**; and
> means for electrically contacting the bottom surface of said first region.

Siliconix states that this disputed phrase means "one or more contacts that electrically connects to the top surface of the source region as to permit electric current to flow to or from the source region, or equivalents thereof." Defendants propose that the phrase signifies "one or more contacts, excluding a metal layer overlaying the gate region, that electrically contact the top surface of the third region." The September 2004 order construed this phrase as Siliconix now requests (Order at 14).

This is a means-plus-function claim phrase, as both parties agree. Such phrases are governed by 35 U.S.C. 112 ¶ 6. In construing a means-plus-function claim phrase, the recited function within that limitation must be first identified. *ACTV, Inc. v. Walt Disney Co.*, 346 F.3d 1082, 1087 (Fed. Cir. 2003). Then, the written description must be examined to determine the structure that corresponds to and performs that function. *Ibid.*

The claimed function, as the parties agree, is a means for electrically contacting the top surface of the source region. The question remaining is the corresponding structure (or structures) that performs that function *according to the specification*. Several passages from the '785 specification are significant (col. 1, lines 31–34).

> Source regions 13a and 13b are electrically tied to body regions 12a and 12b by metal contacts 18 and 19.

Furthermore (col. 1, lines 69–col.2, lines 3)

> Source regions 1a and 21b are electrically tied to body regions 21a and 20b, respectively, by metal contacts 18 and 19 which are also electrically tied together.

Finally (col. 4, lines 57–60):

> The source/body contact shown schematically in FIG. 3 is fabricated using prior art techniques, and in cross section typically appear as shown in FIG. 1.

These passages indicated the possible structures for performing the above-stated function. Figures 1–3 of the '785 patent depicted one or more contact points connected to the source

region. Figure 3, *supra*, was described as typically shown as in Figure 1 where metal contacts were depicted as 18 and 19. Thus, 18 and 19 were presumably showing also metal contacts in Figure 3. Figure 3 depicted two metal contacts of forward-hatched area towards on top of the source and body regions.

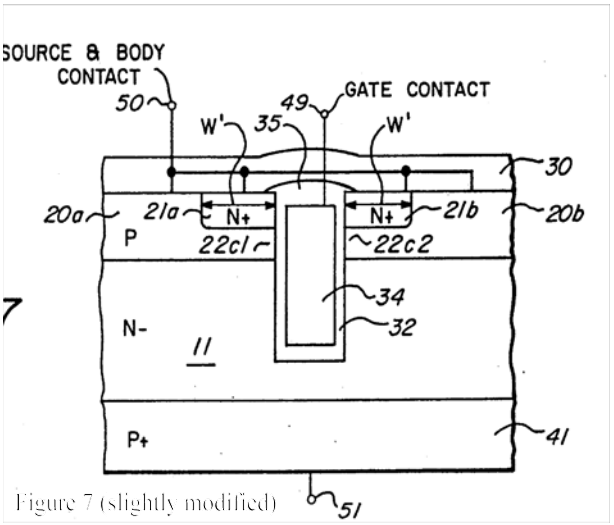

Figure 7 (slightly modified)

Defendants note, however, that the September 2004 order ruled out equivalents containing a metal layer *over* the gate structure. Nothing in the specification taught a metal layer over the gate structure. Figure 3, *supra*, was the closest to any layer of metal contact. Still, Figure 3 showed a disjunction between the two contact points; there was no metal layer over the gate structure. Nor did Figure 7, depicted here, show a metal layer. Instead, layer 30 was described in the specification as a silicon dioxide layer (Col. 3, line 63). The Court cannot change the specification "to correct" any mistakes. *Novo Indus. L.P. v. Micro Molds Corp.*, 350 F.3d 1348, 1354 (Fed. Cir. 2003).

Siliconix contends that even if the specification did not describe a structure containing a metal layer over the gate, the '785 inventor identified such a structure in the prosecution history. The statute and the case law are clear, however, that the list of equivalent structures must be set forth in the *specification*. *See, e.g., Al-Site Corp. v. VSI Int'l, Inc.*, 174 F.3d 1308, 1320 (Fed. Cir. 1999). Nor does the disclosure of such a structure in an incorporated prior-art reference satisfy Section 112(6). As emphasized in the authority relied upon by Siliconix, *Clearstream Wastewater Sys., Inc. v. Hydro-Action, Inc.*, 206 F.3d 1440, 1445 (Fed. Cir. 2000), for a prior-art structure to be included in the meaning of Section 112(6) term, the structure itself must be disclosed in the patent specification. No prior-art structure containing a metal layer over the gate was contained in the specification.

This order modifies the prior construction to specifically exclude purported equivalent structures containing a metal layer over the gate structure. Accordingly, this order construes

"means for electrically contacting the top surface of said third region" to mean "one or more contacts, excluding a metal layer overlaying the gate region, that electrically contact the top surface of the third region, or equivalents thereof."

4. "ELECTRICALLY CONDUCTIVE REGION"

The phrase "electrically conductive region" appeared in claims 1 and 2 of the '785 patent. For example, claim 1 described "an **electrically conductive region** electrically contacting said source and body regions" (col. 7, lines 8–9) (emphasis added). This phrase was not construed in the September 2004 order.

Both parties agree that this phrase is understandable according to its plain and ordinary meaning. Defendants, accordingly, propose the phrase be left as is. Siliconix, however, argues that this phrase must be interpreted in light of the interpretation of the means-plus-function term above.

This order agrees with defendants that this phrase should be left as is. This phrase is not contained in the means-plus-function claim term interpreted above, thus the construction of the two phrases is independent. It will be less confusing for the jury if this phrase is left alone. As stated above, a phrase need not be construed where the ordinary meaning is evident to the jury. *See U.S. Surgical Corp.*, 103 F.3d at 1568.

CONCLUSION

The foregoing claim-construction ruling shall govern all subsequent proceedings herein.

IT IS SO ORDERED.

Dated: June 8, 2006

WILLIAM ALSUP
UNITED STATES DISTRICT JUDGE